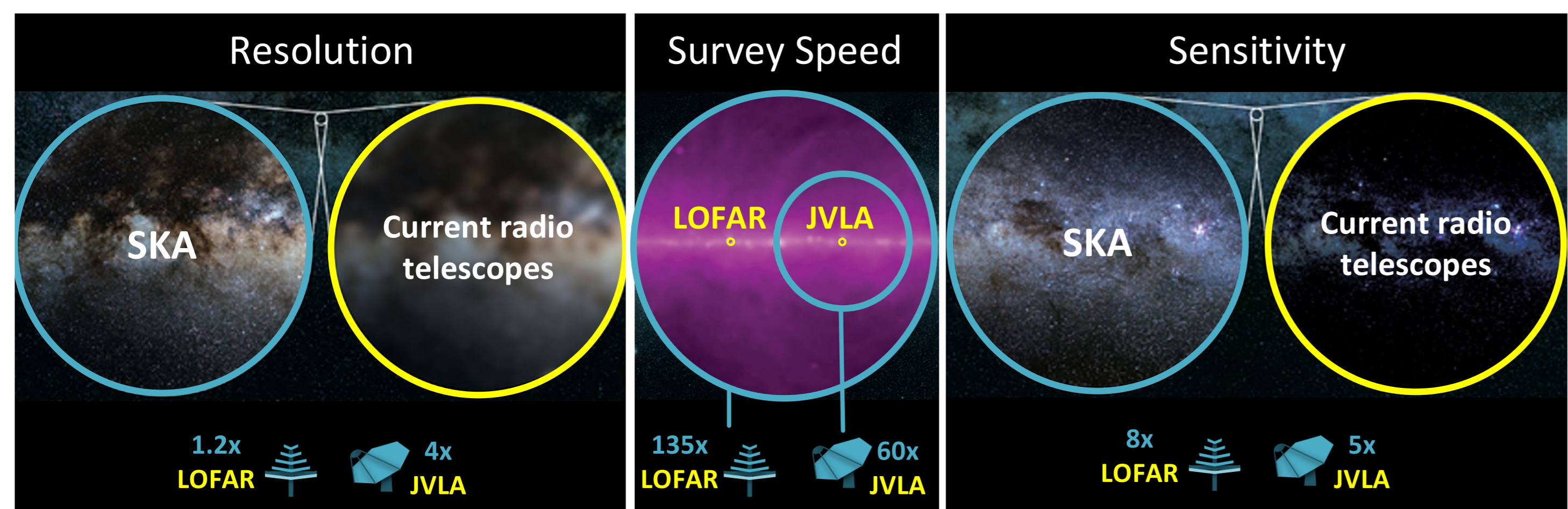


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Enabling Science Beyond Capabilities of Best Telescopes



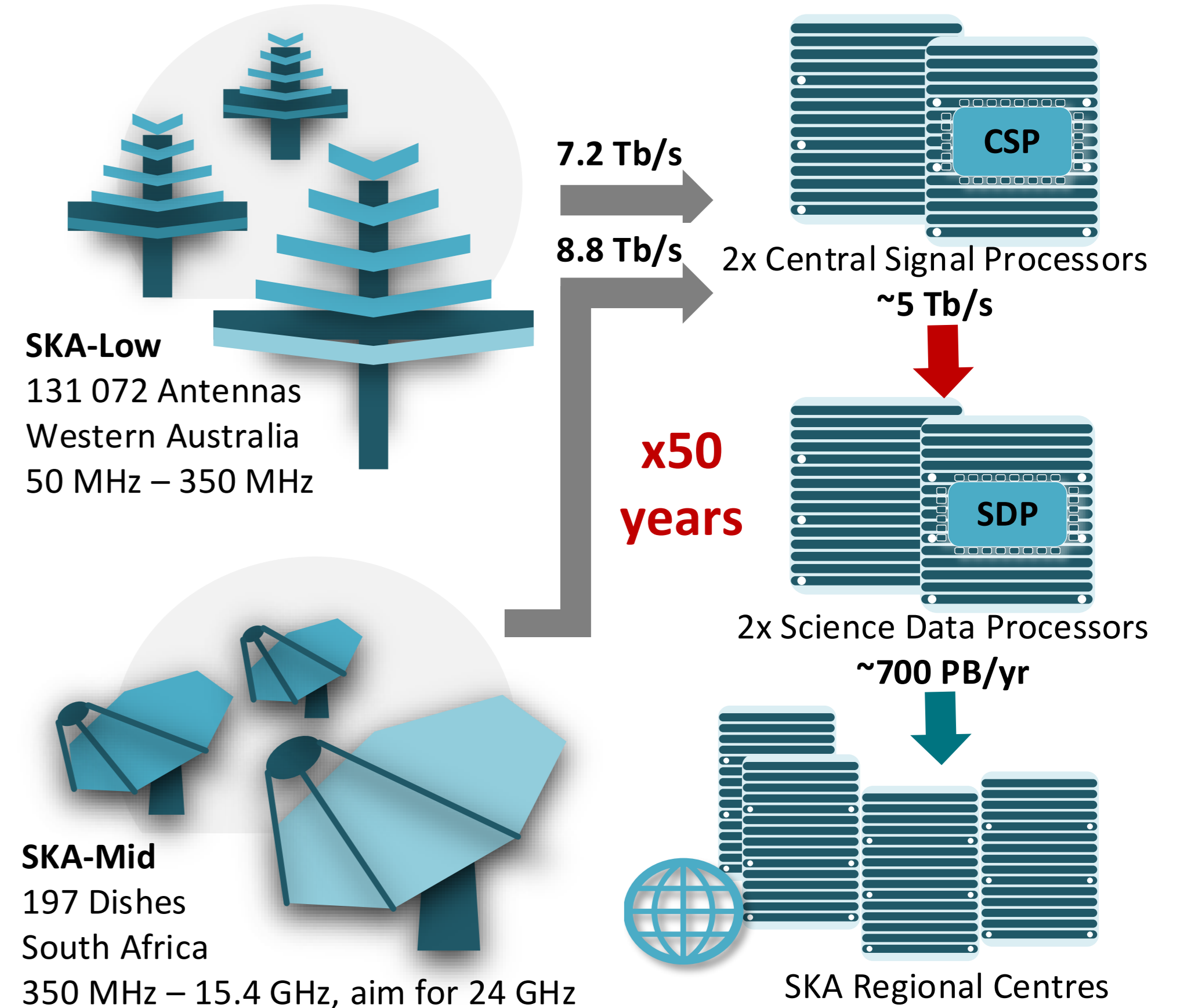
SKA Science Goals Include

Images source: www.skao.int



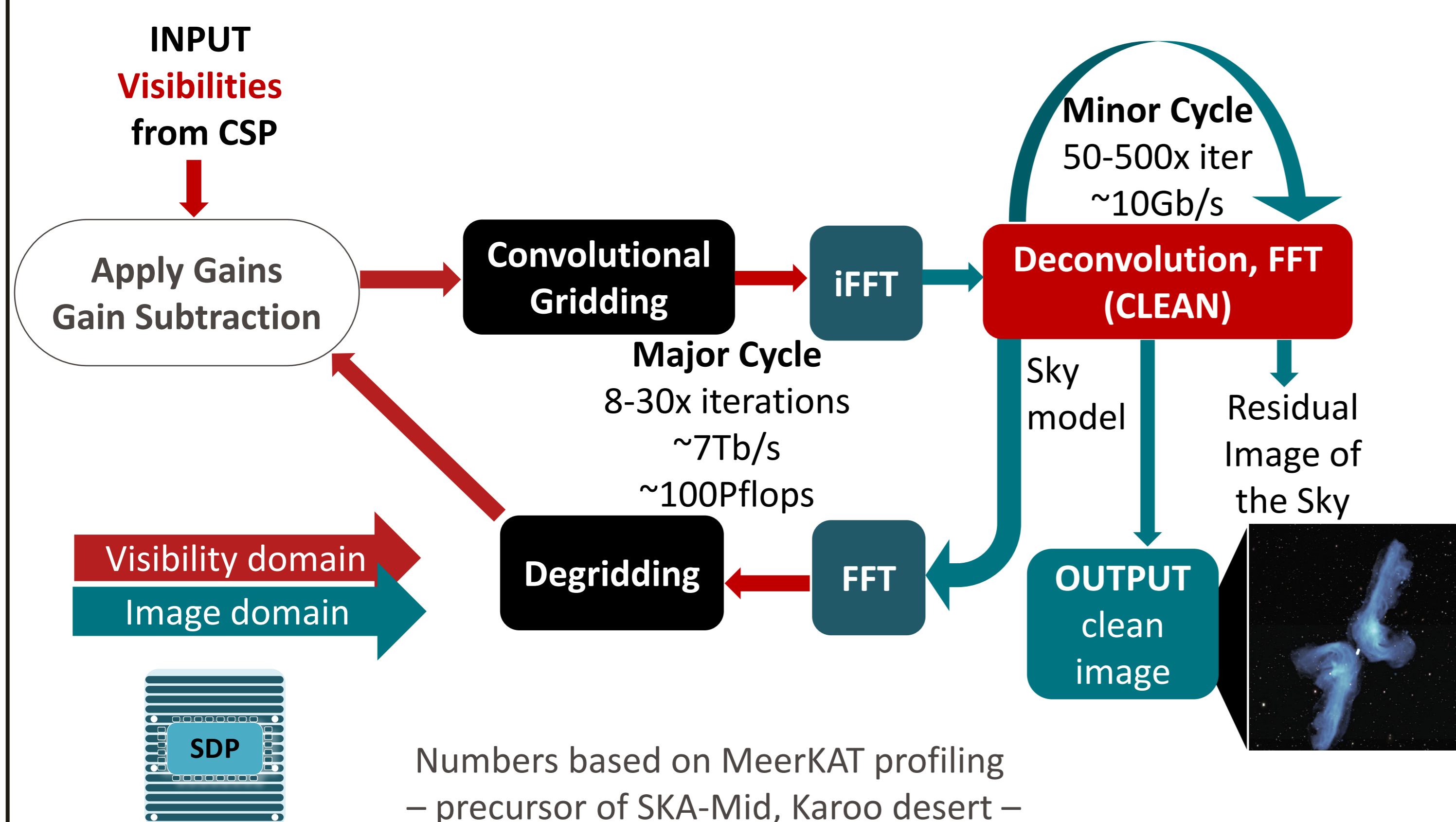
SKAO Consortium

The Square Kilometer Array Observatory in a Nutshell



Energy-Efficient HPC + Big Data Challenge

1 MWatt Budget for 250 PFlops for Science Data Processor



Top 3 Green500 Adastra
 [Power: 0.92 MWatt, 58.021 GFlops/Watts]
 ~Scales to 63 PFlops for 1 MWatt

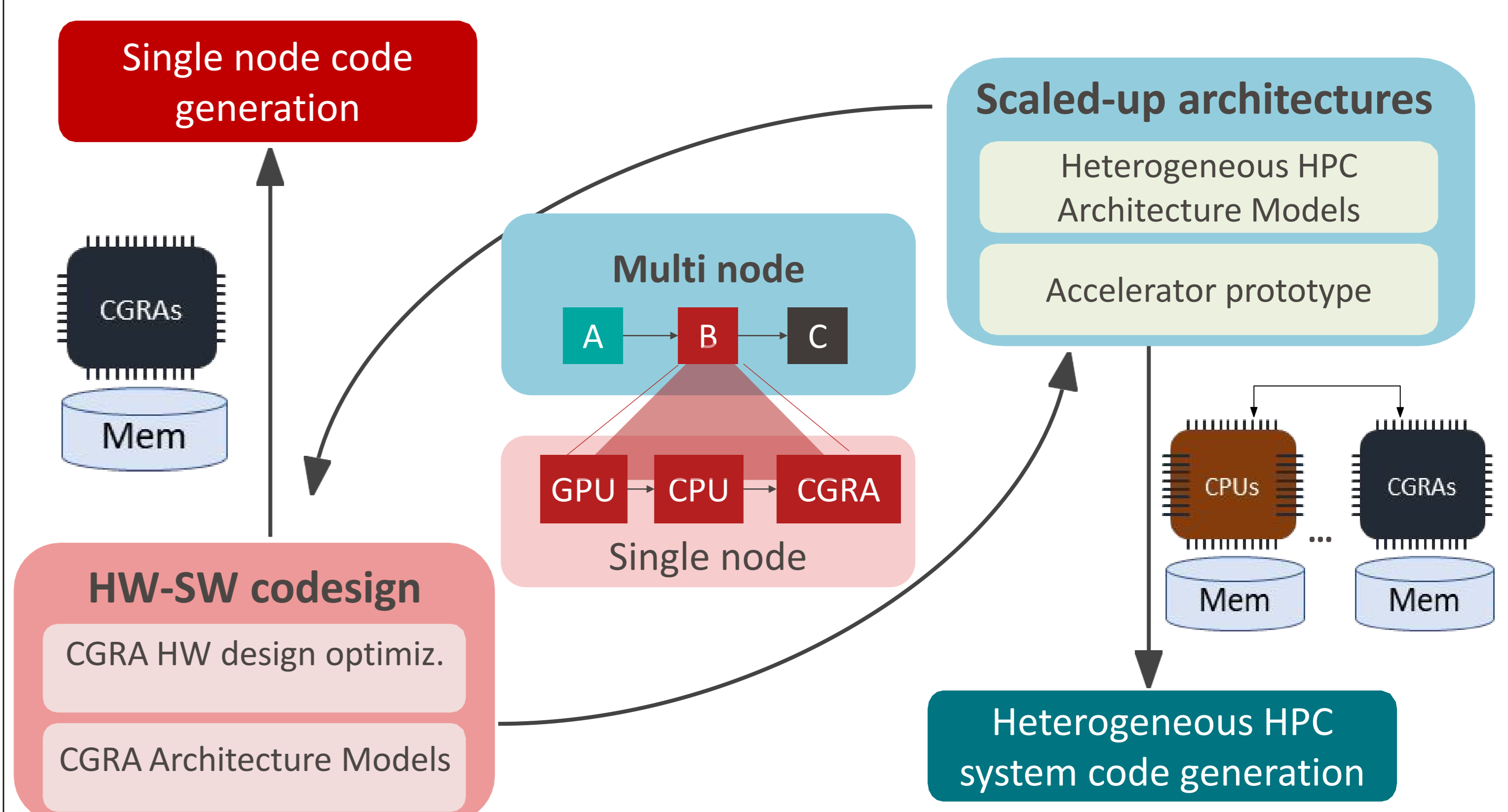
Need Technological Innovations
 4x Energy Efficiency!

Sustainable computing + big data + high throughput

Software pipeline not fixed and evolving

Proposal: Multi-Scale Codesign for Sustainable Acceleration

Heterogeneous execution framework for COTS and domain-specific accelerators



Single node - heterogeneous multiprocessing system integration challenge

- New domain-specific accelerator for interferometry computation
- Methods for heterogeneous computing scheduling to integrate custom design accelerator with commercial off-the-shelf accelerators (GPUs, FPGAs, IPU)
- Parametric architecture: can accommodate different image sizes, accuracy

Multi-node - scalability challenge

- Multi-node scalability of energy efficiency, sustainability, performance & accuracy
- Dynamic workload – many different pipelines
- Highly heterogeneous data center infrastructure
- Extendable multi-node architecture – new types of accelerators

Conclusions

Needs	Business, Research & Innovation Opportunities
Scalable & sustainable HPC for big data	Cloud computing and storage Emissions-aware planning for SKA CSPs, SDPs, and Regional Centres
Real-time requirements	High-throughput technology (I/O, memory, computing)
Old legacy radio-interferometry software	Refactor and scale for modern hardware and HPC
Tradeoffs: programmability, throughput, energy-efficiency	Programmable domain-specific accelerators

Initial seed project between EcoCloud and SKACH

to be extended with new ANR/SNSF project: "SEAMS: Sustainable & Energy Aware Methods for SKA"

Programmable domain-specific accelerators (e.g, CGRA)

Mature, production-level open-source design frameworks
 Hardware IPs: high bandwidth memories, PCIe/CXL
 SwissChip, EuroPractice flagship demonstrators
 Heterogeneous execution frameworks



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